(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 556 820 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **93102547.2**

(51) Int. Cl.[5]: **H01L 21/336**, H01L 27/12

(22) Date of filing: **18.02.93**

(30) Priority: **20.02.92 US 839268**

(43) Date of publication of application:
25.08.93 Bulletin 93/34

(84) Designated Contracting States:
DE FR GB IT

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(54) Process for producing a solid state radiation detector.

(57) A process for producing an array of solid state radiation detectors includes depositing on a substrate one or more layers of silicon-based materials and then depositing a metal layer overlying silicon-based substance. The metal layer is formed into an array of metal layer regions, and then the metal layer is used as a mask to remove exposed adjacent silicon-based substance layers thereby forming an array of silicon-based substance layers that are aligned with the array of metal layers for forming an array of photosensitive sensing devices. The process of the present invention reduces the number of microlithography steps that are used in forming an array of layered amorphous silicon photosensitive devices.

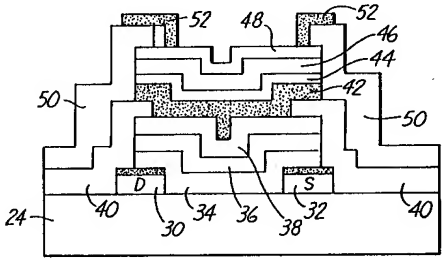

Fig. 13

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The present invention relates to x-ray sensing detectors, in particular, it relates to a process for fabrication of such detectors.

Efforts have been made to replace x-ray film in radiology through the use of x-ray intensifiers, video cameras, displays, and non-film detectors. One such system employs a scintillation crystal to convert x-rays to corresponding visible light radiation, "Digital Slot Radiography Based on a Linear X-Ray Image Intensifier and Two-Dimensional Image Sensors," Beerlage, Levels, and Mulder, SPIE Vol. 626 Medicine, XIV/PACS IV 161-169 (1986). A photodetector is then used to generate an electrical signal corresponding to the intensity of the visible light radiation. The electrical signal from the detector is converted to digital data and stored in a memory device or electrically displayed, such as on a cathode array tube.

Solid state detectors have also been used in x-ray astronomy. One such detector system was reported in "Multi-Element Self-Scanned Mosaic Sensors," Weimer et al, IEEE Spectrum, March 1969, pages 52-65. The system included an array consisting of a matrix of photodiodes which are charged by light to produce electron-hole pairs.

The Catchpole et al U.S. Patent 4,675,739 describes an incident radiation solid state sensing array made of photosensing elements. Each photosensing element includes back-two-back-diodes, one a photo responsive diode and the other a blocking diode. Each of the diodes has an associated capacitance formed by its electrodes. The magnitude of the charge remaining on a given capacitor is sensed and relates back to the intensity of the incident radiation impinging upon the photosensitive diode. Furthermore, in such a linear photodiode array, the scanning time is so long that real time read-out is made impractical. In addition, the linear photodiode array has to be moved to obtain a two-dimensional image.

Another solid state sensing array includes charge-coupled devices. Charge-coupled devices have a layer of relatively conductive semi-conductor material separated from a layer containing electrodes by an insulator in a two-dimensional image sensing array. However, charge-coupled devices can presently be produced at a format of only less than one inch by one inch. Larger formats of arrays have charge transfer problems due to the number of defective devices that can exist in one line of the array. A defective device in one line of the array can result in a charge not being transferred through that line in the array.

The Nishiki et al U.S. Patent 4,689,487 describes the use of a large area solid state detector (40cm X 40cm). This solid state detector includes pixels in 2,000 X 2,000 matrix form. Each pixel consists of a photodiode conductively connected in parallel to a capacitor which are both then conductively connected to the drain of a metal oxide semiconductor field effect transistor (MOSFET). The photodiodes are of a polycrystalline or amorphous silicon material.

The Berger et al U.S. Patent 4,810,881 describes an amorphous silicon detector of 36cm X 43cm. Each pixel in the detector includes an amorphous silicon diode that is conductively connected in series to a capacitor which in turn are both then conductively connected to the drain of an amorphous silicon-based junction field effect transistor.

In any fabrication process of making large area solid state detectors, the number of microlithography masking steps plays a critical role in determining the yield of usable detector devices, and hence the commercial viability of such devices. Solid state detector devices that include photodiodes and thin-film transistors (TFTs) require a high number of microlithography masking steps. For example, 16 masking steps may be required to produce a DRAM (Dynamic Random Access Memory) device and nine to ten steps to produce a liquid crystal display device. The yield Y for such devices is proportional to Y^n, where Y is the yield for each individual masking step, and n is the number of masking steps. The yield may also be defined by $Y=e^{-\sqrt{AD}}$ where A is the chip area and D is the defect density defined as defects per square centimeter. A high number of microlithography steps will cause more defects and large area will create a lowering in yield. Principles of CMOS VLSI Design, Neil Weste, and Kamran Eshraghian, Addison-Wesley Publishing Co., pg. 156. It will be appreciated that the alignment during masking must be exact due to the small area of each pixel, for example, 85μm X 85μm. Misalignment of the masks can occur easily and result in a short in the device.

The present invention includes a process for producing an array of thin film solid state detectors. The process includes depositing on a substrate one or more layers of a silicon-based substance. A metal layer is then deposited overlying the silicon-based substance layers. An array of metal layer regions is formed in the metal layer by removing selected areas of the metal layer thereby exposing selected layers of the silicon-based substance. Then using the metal layer regions as a mask, selected areas of the silicon-based substance layers are removed to form the array of sensing devices thereby automatically aligning the silicon-based substance layers with the metal layer.

The invention is described in detail in connection with the drawings in which:

Figure 1 is an exploded perspective view of an x-ray detector of the present invention,

Figures 2 through 13 are sectional views of the process of the present invention forming one pixel unit of the detector array of the present invention,

Figures 14 through 23 are sectional views of another embodiment of a pixel unit of an array formed by the process of the present invention.

The present invention includes a process for producing an array of thin-film radiation detectors using a greatly reduced number of microlithography steps. In the process of the present invention, one or more layers of a silicon-based substance are deposited on the substrate. By silicon-based substance is meant amorphous silicon, polysilicon, single crystal silicon, or silicon alloys. Silicon alloys include alloys such as silicon nitride, silicon oxide, silicon carbide, and the like. A metal layer is then deposited adjacent the layers of silicon-based substance. Selected areas in the metal layer are then removed exposing selected areas of the silicon-based substance layers. Using the metal layer as a mask, the selected areas of the silicon-based substance layers are removed to form the array of sensing devices of the present invention.

The process is particularly useful in forming an x-ray sensing detector 12 as illustrated in Figure 1 having a large detection area such as 14 inches by 17 inches. The detector 12 includes a luminescent layer 14, an array layer 16 of either amorphous silicon Schottky barrier diode, amorphous silicon p-i-n diode, or amorphous silicon photoconductors, or direct x-ray sensors having amorphous selenium wherein luminescent layer 14 is not required, and a polysilicon or single crystal silicon thin-film transistor (TFT) array layer 18. The detector further includes real-time read-out circuitry 20. The luminescent layer 14 converts incident x-rays to corresponding visible light radiation. The array 16 generates an electrical signal corresponding to the intensity of light from the luminescent layer 14. Current generated in the array 16 is fed to the electrodes of associated TFTs in the array 18.

The pixels forming such an array are typically 85μm X 85μm in area. Alignment of the various layers in the TFTs and the array 16, and alignment of the array 16 with respect to the TFTs is essential for a commercially viable device that produces an image with satisfactory resolution. The greater the amount of defective pixels in such a device, the poorer the resolution of the image. In addition, alignment of the layers in each pixel results in an active area in each pixel that is greater than the active areas in pixels produced under prior art methods. The sequence of microlithographic steps that were used in prior art methods resulted in each subsequently formed layer being smaller in area than the layer below in order to minimize alignment problems. Since the process of the present invention automatically aligns the layers as discussed above, the resulting active area of each pixel is greater.

An example of the process of the present invention that produces the sensing device of Figure 1 is illustrated in Figures 2 through 13. First, a metal such as chromium is deposited as layer 22 on a coated silicon wafer substrate 24 as illustrated in Figure 2. Other substrates, such as glass, SiO_2, or quartz, may also be used. The chromium is deposited in a layer approximately 100 nm to 300 nm thick by sputtering. Other metals such as tantalum or molybdenum in thicknesses ranging from 100 nm to 300 nm are also suitable. Other metals may be deposited by using E-beam evaporation or thermal resistance evaporation. On top of the metal layer 22 is deposited a layer 26 of n-type doped amorphous silicon (n^+-a-Si:H) at a thickness of 50 nm. The n^+-a-Si:H is deposited preferably using plasma-enhanced chemical vapor deposition (PECVD). However, other techniques such as low pressure chemical vapor deposition (LPCVD), electron cyclotron resonance chemical vapor deposition (ECRCVD), or sputtering a silicon target in hydrogen and argon atmosphere may also be used. A photoresist layer 28 is then spin coated on the n^+-a-Si:H layer, and a conventional microlithographic procedure is then used to form the drain region 30 and source region 32 on the substrate 24 as illustrated in Figure 3. This microlithographic step is also used to form the source and drain lines and contact pads (not shown).

On the formed drain and source regions 30 and 32, an undoped amorphous silicon layer 34 (a-Si:H) of 100 nm to 500 nm in thickness using PECVD is then deposited as illustrated in Figure 4. On top of the undoped amorphous silicon layer 34, a dielectric layer 36 of SiN_x of 200 nm is deposited. The deposition of SiN_x is done through the use of PECVD. The dielectric layer 36 can also be SiO_x or SiN_x/SiO_x or Ta_2O_5 and can be formed by either LPCVD, ECRCVD or sputtering. On the dielectric layer, a layer 38 of platinum 100 nm in thickness is deposited using conventional sputtering techniques. Other metals such as tantalum, molybdenum or tungsten ranging from 100 nm to 300 nm in thickness may also be used. The stacked layers 34, 36, and 38 are then annealed using furnace annealing techniques in a nitrogen atmosphere at 600 °C for 15 hours to crystalize the silicon layers and to enhance the dielectric properties of the layer 36. The annealing may also be done using rapid thermal annealing techniques at 600 to 700 °C in an inert atmosphere such as argon or nitrogen for three to 15 minutes. Optionally E-beam annealing or laser annealing can also be used.

A photoresist layer 37 is then spin coated on the platinum layer 38 and conventional microlithographic techniques to form a pattern in the platinum layer 38 to remove selective areas of the layer 38. The selected areas are preferably removed by sputter-etch in an argon atmosphere. The remaining areas of the layers 38 and 37 serve as a mask, as best illustrated in Figure 5, for the removal of selected areas of the dielectric layer 36 and the amorphous silicon layer 34. After removal of the selected areas of layers 34 and 36, the photoresist layer 37 overlying the layer 38 is removed. As can readily be appreciated, the layers 34, 36, and 38 are automatically aligned due to the use of layer 38 as a mask as illustrated in Figure 6.

Prior to formation of the photodiode, the layers 34, 36, 38, and the drain region and source region are insulated by the deposition of an insulating layer 40, as illustrated in Figure 7. The insulating layer 40 is preferably a triple layer containing a first layer 200 nm in thickness of SiN_x, a second layer 200 nm in thickness of SiO_x, and a third layer 200 nm in thickness of SiN_x. The thickness of the insulating layer may range from 400 nm to 800 nm.

A photoresist layer 42 is then deposited on the insulating layer 40 and a microlithographic masking step is then used to open a via hole over each TFT which will subsequently be used to conductively connect the TFTs with the photodiodes in the array, as illustrated in Figure 8. Next, the photodiode 41 is formed over the TFT 39, as illustrated in Figure 9. A chromium layer 42 of 100 nm thickness is deposited by sputtering. An n-type doped amorphous silicon layer 44 (a-Si:H) of 50 nm thickness is then deposited using PECVD. Next, an undoped amorphous silicon (a-Si:H) layer 46 of 400 nm to 500 nm thickness is deposited on the layer 44. Lastly, a platinum layer 48 of 15 nm thickness is deposited preferably using known sputter-etch technique on top of the layer 46 to complete the layers forming the photodiode 41.

A photoresist layer 50 is then spin coated on the platinum layer and microlithography is used to pattern the platinum layer, removing selected areas with the remaining areas overlying the TFT 39, as best illustrated in Figure 10. The remaining platinum areas of the layer 48 are then used as a mask to remove selected areas of layers 42, 44, 46 to form the photodiode 41, as illustrated in Figure 11. Using the remaining areas of the platinum layer 48 as a mask, automatically aligns remaining areas of layer 42, 44, 46 beneath the platinum layer with the platinum layer. As discussed previously, prior art techniques required the use of multiple microlithographic steps between the depositions of each layer. Using multiple microlithographic steps required exact alignment of the masking of each layer. Even with exact alignment attempts, defects, such as, the top platinum layer 48 and the bottom electrode layer 42 being slightly misaligned can occur causing shorts in the device.

Although sputter-etching of the platinum layer 48 is preferred, other techniques such as wet etch using aqua regia or lift-off techniques may also be used. The n+-type a-Si:H layer 44 and the undoped a-si:H layer 46 are etched using preferably reactive ion etching (RIE). Wet etch techniques can also be used. Aqua regia etching is not as preferred as sputter-etching, since aqua regia etching suffers from the disadvantage of attacking other layers and just as quickly or even faster than the platinum. Lift-off techniques give imprecise etch definition and surface contamination, which results in a device that is somewhat inferior to the one that is made by sputter-etching. In the use of sputter-etching, the photoresist layer should be left on the platinum until the underlying layers have been etched to form the device. The photoresist helps protect the platinum layer 48 during the etching of the underlying layers 44 and 46. The layers 44 and 46 may be removed by wet or dry etching while the chromium layer 42 is removed by wet etching.

Platinum is preferred as the top layer for the photodiode. In addition, although other metals have been mentioned for use in the gate, source, and drain regions of the TFT, platinum can also be used. Platinum is preferred since it is an inert material and is not easily attacked by etching chemicals, which makes platinum a preferred metal for use as a mask in the process of the present invention. In addition, platinum has a very high Z (Z = 78), which aids in protecting the layers underneath the platinum layer from x-ray radiation. X-ray absorption is a function of Z^5. Metals having Z of at least 73, and preferably 74 or better, aid in x-ray absorption.

After the photodiode has been formed, annealing may be done in a hydrogen atmosphere at 0.5 to 2 Torr at approximately 300 °C for one to three hours to reduce the defect densities at the platinum/a-Si:H interface. Platinum layers as thick as 30 nm have been used successfully.

Alternatively, a p-i-n diode may also be formed over the TFT 39 using the techniques described above instead of a Schottky barrier diode. Initially, a layer of chromium approximately 100 nm is deposited over the TFT. Next, an n-type doped amorphous silicon layer approximately 10 nm to 50 nm is deposited on the chromium, with an undoped amorphous silicon layer approximately 400 nm to 500 nm deposited on the n-type doped amorphous silicon layer. Next, a p-type doped amorphous silicon layer is deposited on the undoped amorphous silicon layer of 10 nm to 50 nm in thickness. Alternatively, the p-type doped amorphous silicon can be amorphous silicon carbide (a-SiC:H). An

Indium Tin Oxide (ITO) layer of 100 nm to 200 nm is then deposited on the p-type layer. The order of the p and n layers, of course, can be reversed. The ITO layer is patterned in a similar manner as the platinum layer 48 discussed with respect to the diode 41. After the ITO layer has been patterned and selected areas removed, the ITO layer is then used as a mask to wet or dry-etch the p-i-n or n-i-p layers with the chromium layer being wet-etched last. Other materials such as amorphous silicon-based alloys, single crystal silicon, copper indium diselenide, and other materials known in the art for photodiodes may also be used.

Whether a Schottky barrier diode has been formed or a p-i-n or an n-i-p diode, a top insulating layer 50 is deposited on the diode as illustrated in Figure 12. The insulating layer 50 similar to the insulating layer 42, discussed previously, preferably includes a first SiN_x layer approximately 200 nm, a second SiO_x layer of 200 nm thickness, and a third SiN_x layer of 200 nm thickness. The layer 50 acts as an isolation layer. Microlithography is used to expose the platinum layer 48.

Next, an aluminum layer 52 doped with one percent silicon of approximately 300 nm to 1μm in thickness is deposited on the insulating layer 50 and the platinum layer 48 as illustrated in Figure 13. The layer 52 is then masked using microlithography to define a conductive line.

X-ray sensitive phosphor for use in the detector of the present invention may be chosen from those well-known in the radiographic art for use in intensifying screens. Such phosphors include gadolinium oxysulfide doped with terbium or europium, yttrium oxide, calcium tungsten, barium, fluorochloride doped with europium, barium sulfate or strontium sulfate doped with terbium or thulium or dysprosium, and zinc sulfide or with cesium iodine doped with thallium. The phosphor may be situated individually over each pixel in microcolumns. The individual microcolumn arrangement confines the scattered emitted light to the area of the associated pixel. Although conventional screens can also be used with the present invention, the use of such a screen results in some spreading of the emitted light which causes a reduction in the image sharpness.

The use of columnar phosphor results in greater image sharpness since the emitted light is confined to the column area. In addition, since the scattered emitted light is confined, the thickness of the phosphor layer can be increased without loss in image sharpness. Increasing the thickness of the phosphor provides greater absorption of incident x-rays thereby improving the sensitivity of the detector.

Techniques for producing columnar phosphor are known in the art. European patent application Publication 0 175 578 describes the use of columnar phosphor layers selected from barium sulfate doped with terbium or thulium or dysprosium, strontium sulfate doped with terbium or thulium or dysprosium and alkylhalides. Such phosphor layers may be formed by vacuum evaporation, sputtering, or other vacuum deposition techniques known in the art. Columnar phosphor screens including oxysulfides of gadolinium or lanthanum are described in U.S. Patent 4,069,355. Such structured phosphors are made by vapor deposition techniques. Columnar structured phosphors can also be formed by evaporating cesium iodine doped with thallium on the detector.

A metal-oxide-semiconductor field effect transistor (MOSFET) may be substituted for the thin film transistor to produce the device of the present invention. To produce the MOSFET using the process of the present invention, the substrate (which is silicon wafer coated with 1-3μm of thermal oxide for insulating) is coated with an silicon layer of 100 nm to 1.5 μm in thickness using LPCVD or PECVD. Silicon, either in an amorphous state or in a crystalline state is then annealed using furnace annealing, rapid thermal annealing, E-beam annealing, or laser annealing to form large grain size polycrystalline or single crystal silicon. The crystallized silicon layer is then patterned into islands using microlithography. A 100 nm thickness silicon oxide layer for the gate is grown on the patterned crystallized silicon layer. A polysilicon layer of about 100 nm to 350 nm thick is then deposited by LPCVD. The gate oxide and the polysilicon layer are then etched by microlithography. Ion implantation with phosphorous to a level of 10^{15} atoms/cm^2 is done to obtain n-type characteristics. After implantation, the phosphorous is activated by annealing between 800 to 1,050 °C for 20 minutes. A thin layer of 20 nm to 50 nm of silicon oxide was formed on the polysilicon layer due to the activated annealing process. Using microlithography, via holes for drain and source contact are formed in the silicon oxide. Aluminum doped with one percent silicon is deposited by sputtering to form the drain and source during the same microlithography step using a lift-off technique. Using the process of the present invention, only three microlithography steps are used to form the MOSFET.

The electrical connection between the photosensitive diode and the TFT may be done using any one of three alternatives. The bottom contact of the photosensing diode is connected to the TFT gate, or the bottom contact of the photosensing diode is connected to the drain electrode of the TFT, or the top contact of the photosensing diode is connected to the source electrode of the TFT.

The process of the present invention may also be used to form an array radiation detector in

which the position of the gate of the TFT is initially deposited on the substrate, as illustrated in Figures 14 through 23. Initially, a metal layer 62 of chromium or tantalum of 100 nm to 300 nm in thickness is deposited on a glass substrate 60. Prior to deposition, the glass substrate can be coated with a layer of SiO_2 to prevent contamination of the metal layer such as from sodium leaching from the glass substrate. Layer 62 can be deposited by sputtering, E-beam evaporation, or thermal resistance evaporation. A type photoresist layer is then deposited on the metal layer 62. As illustrated in Figure 15, microlithography is then used to form a gate area 63 from the layer 62.

As next illustrated in Figure 16, a dielectric layer 66 of SiN_x of 100 nm to 300 nm in thickness through the use of PECVD is deposited over the substrate 60 and the gate area 63. On top of the dielectric layer 66 is deposited an a-Si:H undoped layer of 500 nm thickness and a phosphorous doped a-Si:H layer 70 50 nm in thickness is deposited on the layer 68, both layers 68 and 70 being deposited by PECVD. A negative photoresist layer 72 is then spin coated on the layer 70. Using the gate electrode area 63 as a mask, UV light, as depicted by arrows 75, is used to inhibit the development of the areas not covered by the gate 63 permitting the area of the photoresist behind gate 63 to develop. The underlying layers 70 and 68 are etched as illustrated in Figure 17 aligning the layers with the gate area 63. The remainder of the photoresist layer 72 is then removed.

Next, a metal layer 74 of aluminum doped with one percent silicon of 100 nm to 300 nm is deposited by sputtering, and a photoresist layer 76 is spin coated on the layer 74, as illustrated in Figure 18. A second microlithography step is used to expose the a-Si:H layer 68 by etching through the metal layer 74 and the doped a-Si:H layer 72 to form a source region 78, a drain region 80 and respective contact lines (not shown).

Next, after the photoresist layer 76 has been removed, the devices forming the array are covered with an insulating layer 82 of approximately 600 nm of SiN_x, as illustrated in Figure 21. A third microlithographic step is used to form a via hole 84 to the drain region, which is then filled with aluminum doped with one percent silicon 86 and the photoresist (not illustrated) is then removed.

As illustrated in Figure 22, a bottom electrode 88 is then formed in conductive connection to the aluminum silicon plug 86 by depositing a layer (not illustrated) of metal approximately 100 nm to 300 nm and a layer of photoresist. A fourth microlithographic step is then used to form the bottom electrode 88 of the to-be-formed photoconductor.

Next, doped and undoped amorphous silicon layers 90 are deposited on the insulating layer 82 and on the bottom electrode layer 88. A top electrode ITO layer 92 of 100 nm to 200 nm is deposited on the amorphous silicon layers 90 to complete the device.

In the photoconductor/TFT structure of Figures 14-23, the photoconductor can include amorphous selenium, lead oxide, selenium-telluride, or other selenium-based alloy. As an alternative structure, an insulating layer can be added on top of the photoconductor layer 90 or in between the photoconductor layer 90 and the TFT without requiring a microlithography step. Although polysilicon is specifically mentioned for use in constructing the TFT, other materials, such as cadmium selenide, can also be used. The present invention is not limited to one TFT/one photodiode arrangement or one TFT/photoconductor arrangement for each pixel. The pixel can be structured with adding one or more photodiodes, one or more TFTs and/or one or more capacitors and/or one or more resistors.

The present invention is useful for making large area detectors. Such large area radiation detectors are formed by assembling several smaller array containing submodules to create a large module such as 14 inches by 17 inches. In forming the large area modules, the submodules are placed adjacent to each other and are then bonded. However, dead space both physical and electronic is often times created between the submodules. In using the process of the present invention, the dead space between the bottom electrode of the photoconductor or photodiode is virtually eliminated.

First, the thin film transistor is formed on a substrate of each submodule as described previously. The submodules are then positioned in a side-by-side relationship adjacent each other and the bottom electrode of the photoconductor or photodiode is then deposited over the adjacent submodules and then patterned using microlithography to form the individual bottom electrodes of the photodiode or photoconductor. The bottom electrode bonds the submodules together, and provides a common continuous bottom electrode layer for the large area detector. On top of the bottom electrode is deposited the doped and undoped amorphous silicon layers as described previously. The top electrode, preferably a platinum layer, is then deposited, and one microlithographic step as described previously is used to form the photoconductor or photodiode, thus forming the large area detector.

Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the inven-

tion.

Claims

1. A process for producing a solid state radiation detector array of pixels, wherein each pixel of the array includes a photosensor electrically connected to a thin film transistor, the process comprising:
providing a substrate;
depositing on the substrate one or more layers of a silicon-based substance;
depositing a metal layer overlying the silicon-based substance layers;
forming an array of metal layer regions in the metal layer by removing selected areas from the metal layer thereby exposing underlying areas of the silicon-based substance layers; and
removing selected areas from the silicon-based substance layers using the array of metal layer regions as a mask.

2. The process of claim 1 wherein:
depositing a silicon-based substance includes depositing on the substrate one or more layers of a single crystal silicon-based substance; and
removing selected areas from the silicon-based substance includes removing selected areas from the single crystal silicon-based substance layers using the array of metal layer regions as a mask to form thin film transistors.

3. The process of claim 1 or 2 and further including:
forming an array of transistor drain and source regions on the substrate prior to deposition of the silicon-based substance layers and wherein the silicon-based substance layers include a doped and undoped amorphous silicon layer, and a dielectric layer and the array of metal layer regions is positioned adjacent the dielectric layer and serves as an array of gate regions.

4. The process of claim 3 and further including forming an array of photosensitive devices overlying the array of gate regions comprising:
depositing a bottom metal layer in conductive connection with the gate regions;
forming undoped and doped amorphous silicon layers on the bottom metal layer;
forming a top metal layer;
removing selected areas from the top metal layer using microlithography to form an array of top metal layers; and
removing amorphous silicon layers and the bottom metal layer using the array of top metal layers as a mask.

5. The process of any of claims 1 to 4 wherein the metal layer is a first metal layer and is deposited directly on the substrate and is formed into an array of gate regions, and further comprising:
depositing a dielectric layer on the gate region;
wherein the silicon-based substance layers are adjacent the dielectric layer and include a doped and undoped amorphous silicon layer; and
forming a second metal layer on a side of the silicon layers opposite from the dielectric layer and the gate region for use as a drain and source region.

6. The process of claim 5 and further including forming a photosensitive device over the array of gate regions comprising:
depositing a bottom metal layer in conductive contact with either the drain or source region;
forming undoped and doped amorphous silicon layers on the bottom metal layer;
forming a top metal layer overlying the silicon layer;
removing selected areas from the top metal layer using microlithography to form an array of top metal layers; and
removing selected areas of the amorphous silicon layers and the bottom metal layer using the array of top metal layers as a mask.

7. A process for forming a two-dimensional array of solid state radiation detectors, the process comprising:
coating a metal layer on to a substrate followed by coating an n^+-type amorphous silicon layer on to the metal layer;
masking the metal layer and the n^+-type amorphous silicon layer using microlithography to form drain and source regions;
forming sequentially a layer of undoped amorphous silicon, a dielectric layer, and a top metal layer on the drain and source regions;
forming an array of gate regions using microlithography from the top metal layer; and
removing selected areas of the dielectric layer and undoped amorphous silicon layer using the array of gate regions as a mask thereby forming an array of thin film transistors on the substrate.

8. The process of claim 7 and further including:
forming a dielectric layer on the array of

gate regions;

masking the dielectric layer using microlithography to provide an array of holes over the array of gate regions exposing the gate regions;

filling the holes with a metal in conductive contact with respective gate regions;

forming sequentially a layer of chromium on the dielectric layer and in conductive contact with the filled metal holes, a layer of n^+-type amorphous silicon, a layer of undoped amorphous silicon, and a layer of platinum;

masking the platinum using microlithography for forming an array of platinum regions; and

removing selected layers of undoped amorphous silicon, n^+-type amorphous silicon and chromium to form an array of photodiodes overlying the array of thin film transistors.

9. A process for forming a two-dimensional array of solid state radiation detectors, the process comprising:

forming an array, of transistor gate regions on a substrate;

forming in sequence a dielectric layer, an undoped amorphous silicon layer, and an n^+-type amorphous silicon layer over the array of gate regions;

spin coating a layer of photoresist layer and using the array of gate regions as a mask and exposing portions of the photoresist layer not covered by the gate regions to a light source;

selectively etching the n^+-type amorphous silicon layer, undoped amorphous silicon layer, and dielectric layers such that a array of layers is formed in alignment with the array of gate regions;

removing the undeveloped portion of the photoresist layer;

forming a metal layer and then a photoresist layer over the array;

masking the photoresist layer and using microlithography to remove selected areas of the photoresist and the metal layer to form a drain and a source region while also removing a portion of the n^+-type amorphous silicon layer which overlies the array of gate regions to expose the undoped amorphous silicon layer; and

removing the remaining photoresist layer forming a thin film transistor.

10. The process of claim 9 and further including:

depositing an isolation layer over the array;

masking the isolation layer using microlithography to form an array of holes in the isolation layer in conductive connection with respective drain or source regions;

filling the holes with metal in conductive contact with the drain regions;

depositing a bottom electrode layer on the isolation layer in conductive contact with the array of filled holes in the isolation layer;

masking the bottom electrode layer using microlithography to form an array of bottom electrodes;

depositing a doped and undoped amorphous silicon layer on the array of bottom electrodes;

forming a top electrode layer over the doped and undoped amorphous silicon layers;

masking the top metal layer using microlithography to form a array of top metal layer regions; and

using the array of top metal layer regions as a mask to remove selected areas of the doped and undoped amorphous silicon layers to form an array of photosensitive devices overlying the array of thin film transistors.

11. A process for producing a large area radiation detector, the process comprising:

forming submodule arrays, each submodule including an array of thin film transistors;

positioning the submodules in side-by-side relationship;

forming an electrode layer that overlies the thin film transistor arrays of the submodule;

depositing on the bottom electrode layer doped and undoped amorphous silicon layers;

forming a top electrode layer on the amorphous silicon layers;

using microlithography to form an array of top electrode regions overlying the thin film transistors of the submodules;

selectively etching the doped and undoped amorphous silicon layers using the array of top electrode regions as a mask to form an array of photosensitive devices overlying the thin film transistors.

12. The process of claim 11, wherein the doped amorphous silicon layer includes an n^+-type amorphous silicon layer and a p^+-type amorphous silicon layer, and further including:

forming submodules, each submodule including an array of thin film transistors;

positioning the submodules in side-by-side relationship;

forming an electrode layer that overlies the thin film transistor arrays of the submodules, and patterning the electrode layer using microlithography to form an array of electrodes overlying the array of transistors;

depositing a continuous layer of photoconductor; and

forming a top common electrode layer.

13. A solid state radiation detector, producible with a process according to any of claims 1 to 12.

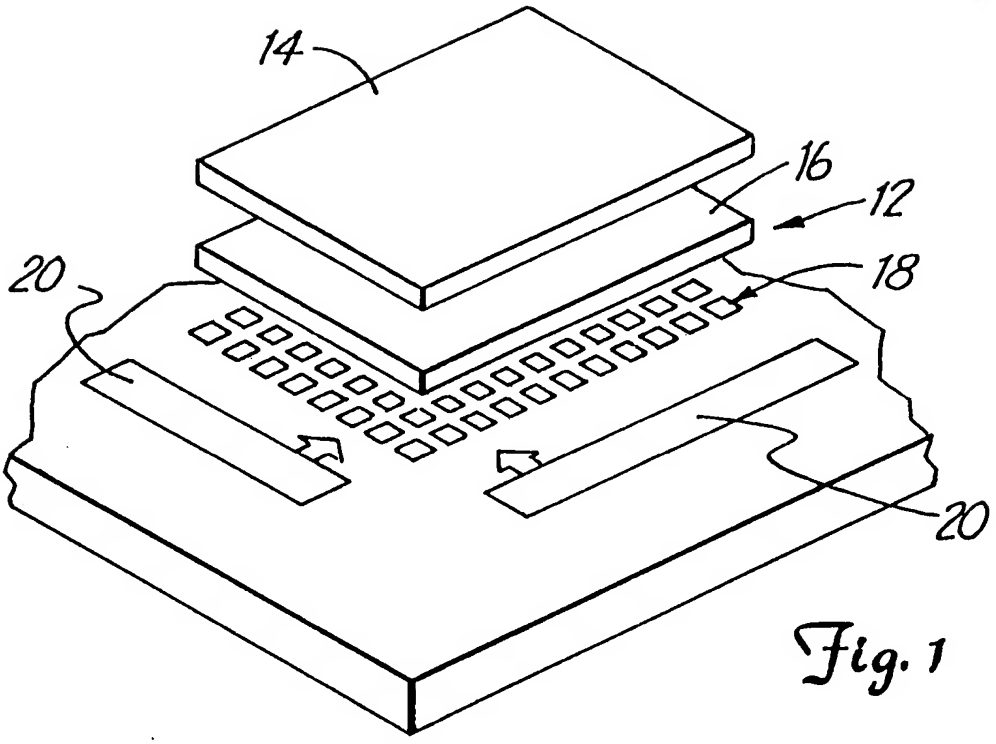


Fig. 1

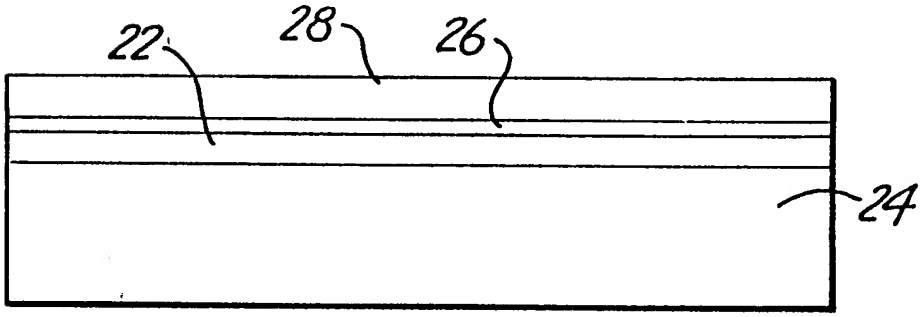
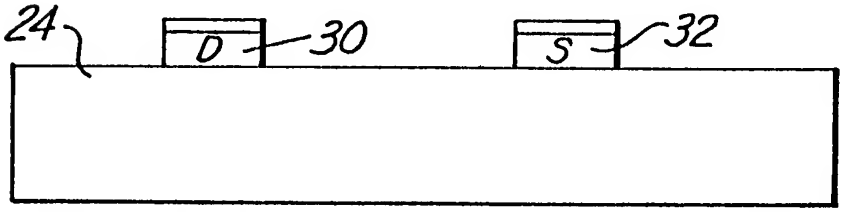


Fig. 2



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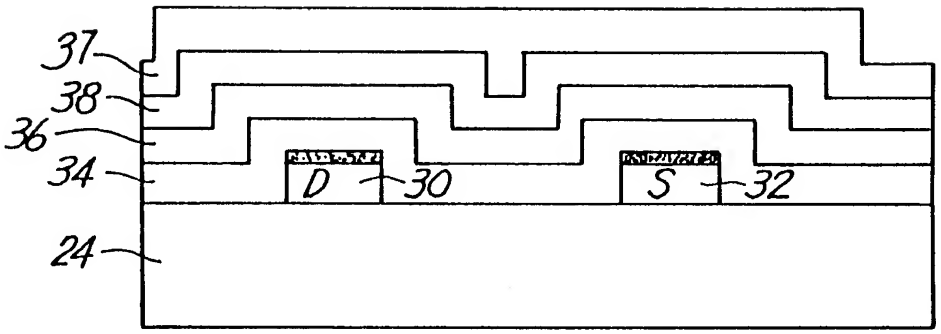

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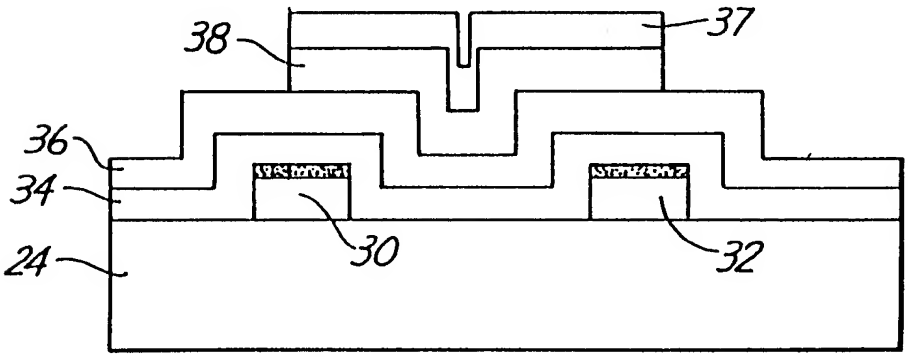


Fig. 5

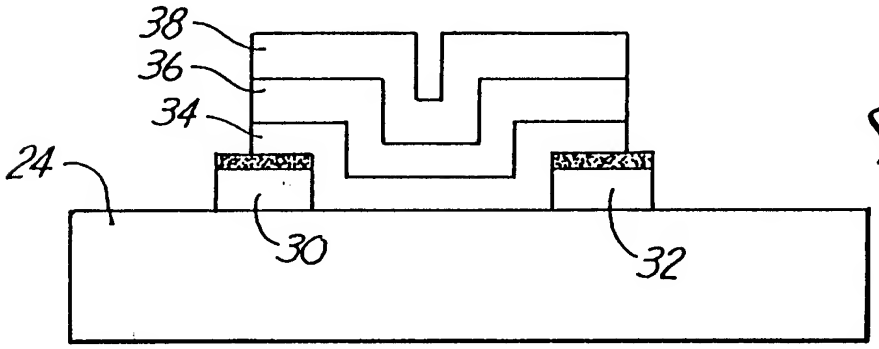


Fig. 6

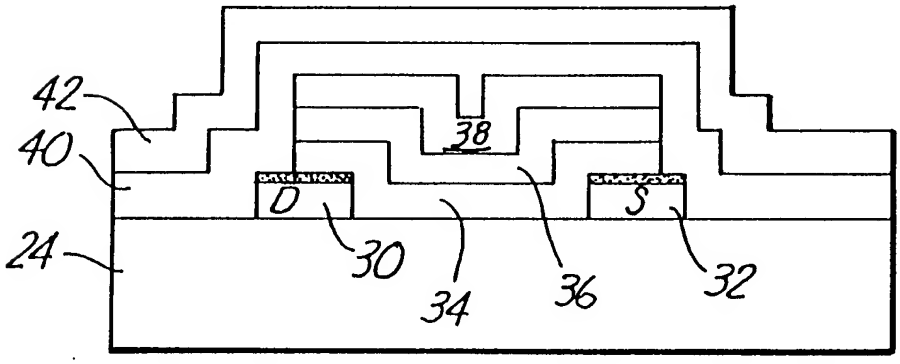


Fig. 7

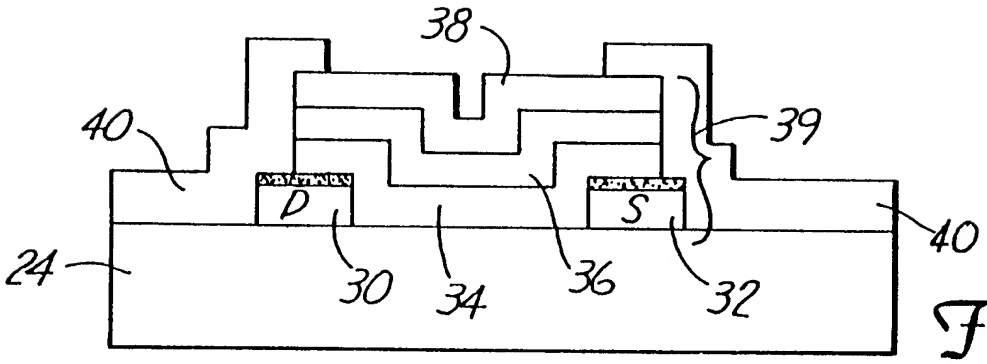


Fig. 8

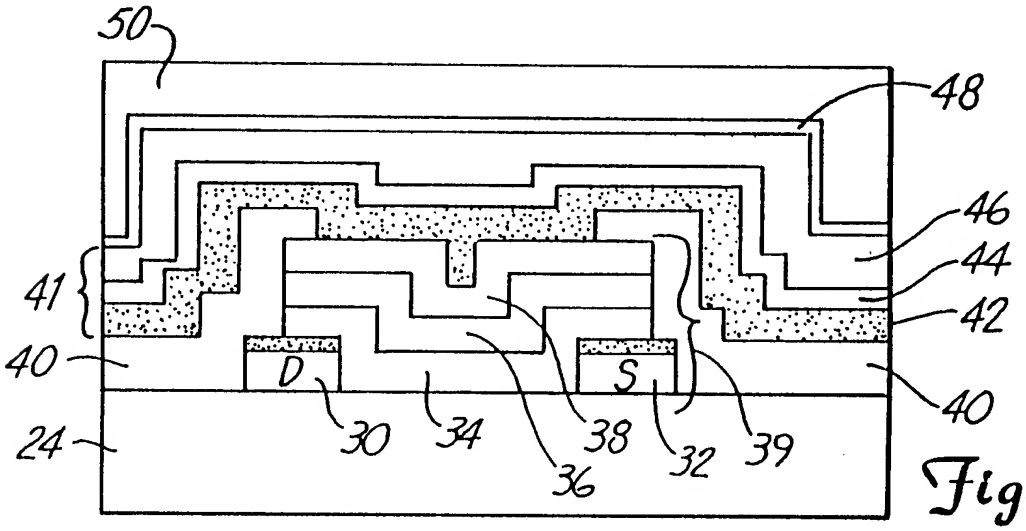


Fig. 9

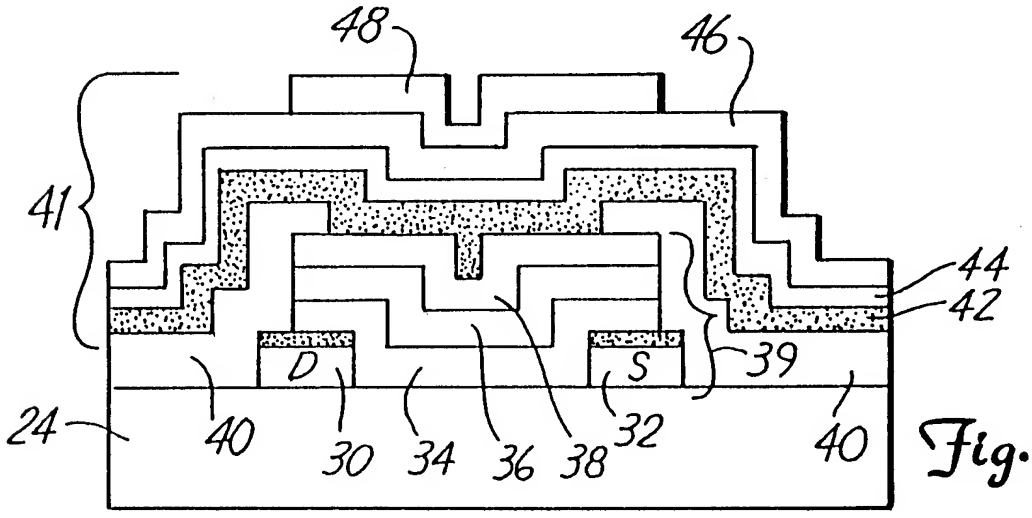
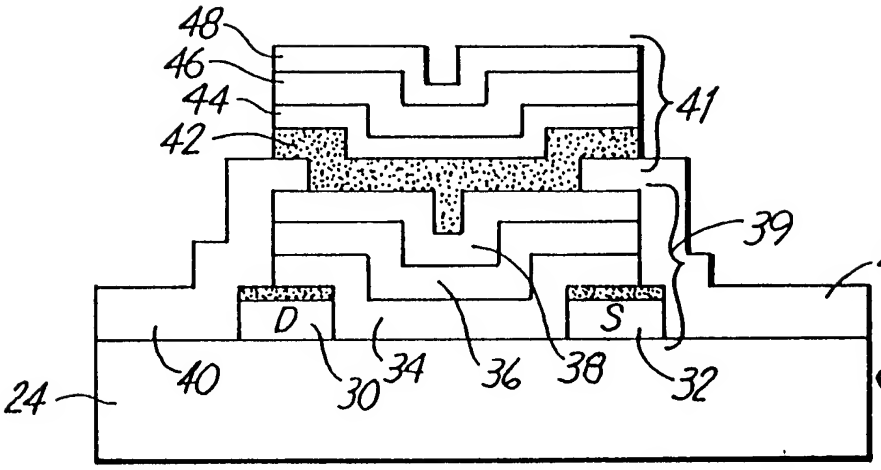


Fig. 10



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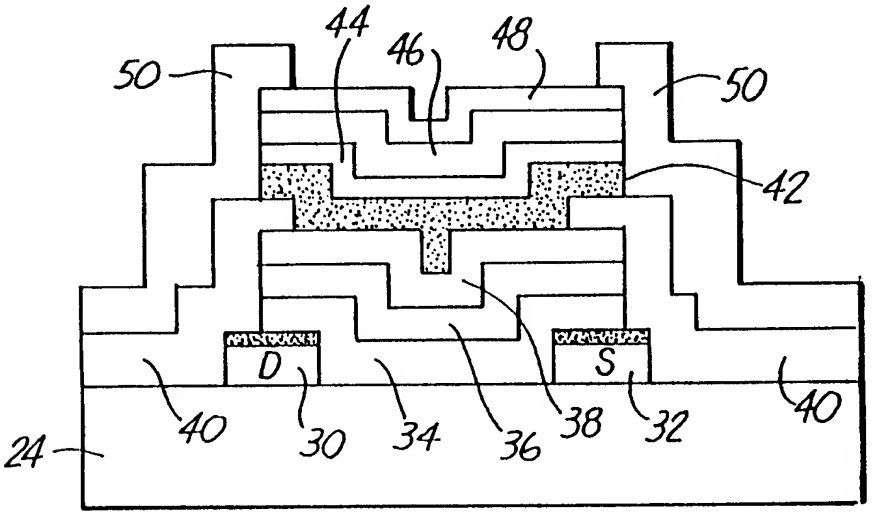


Fig. 12

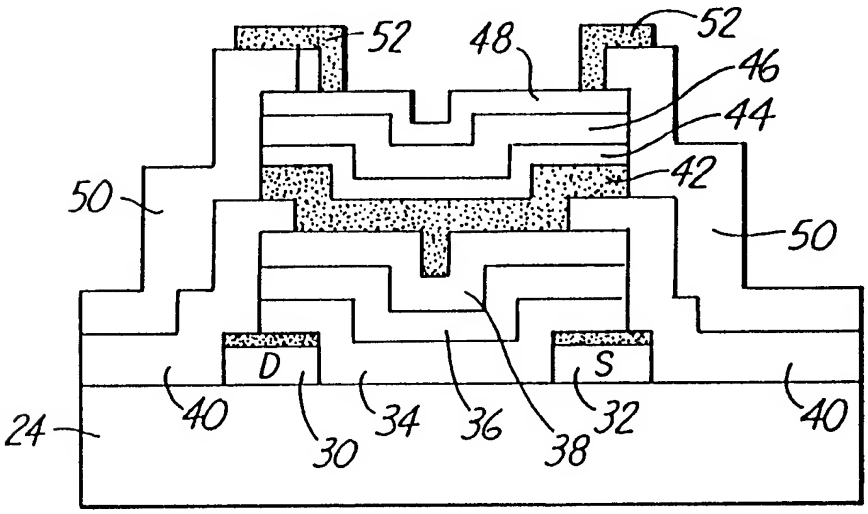


Fig. 13

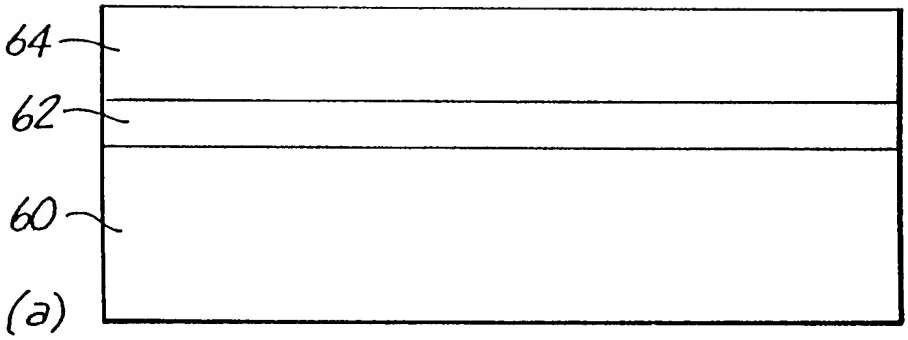


Fig. 14

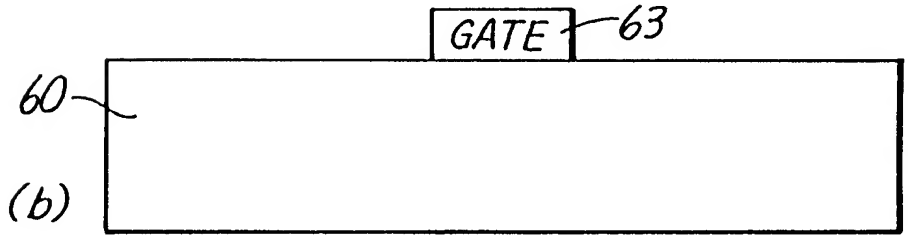
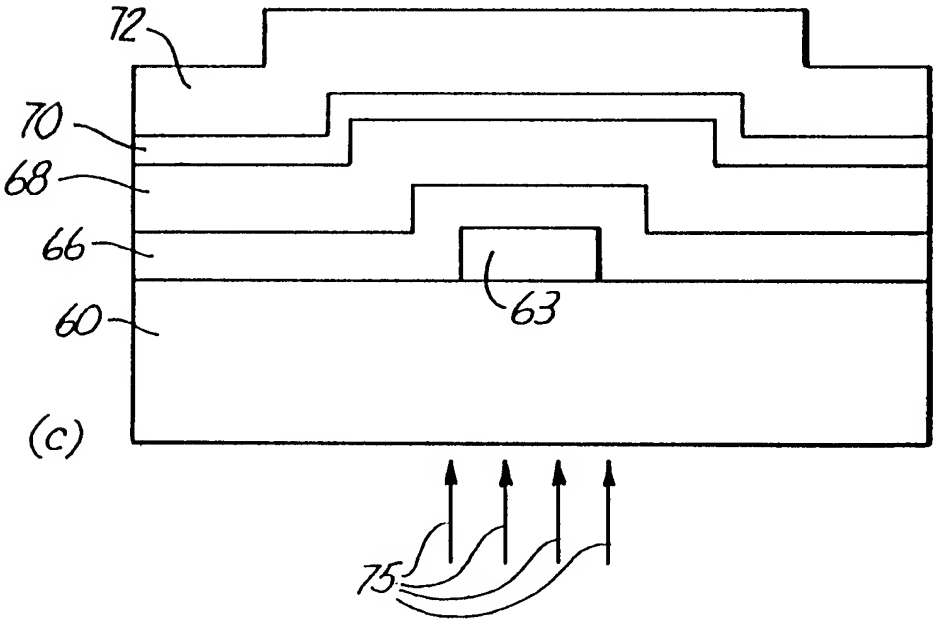


Fig. 15



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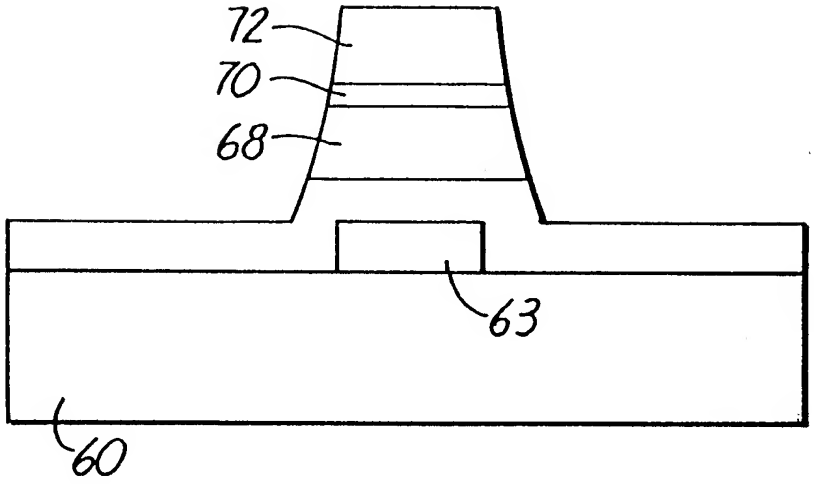

Fig. 17

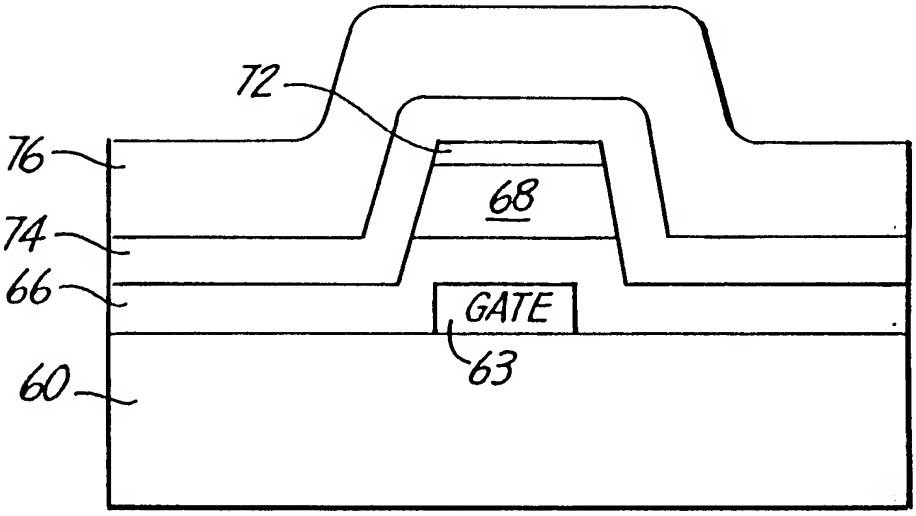

Fig. 18

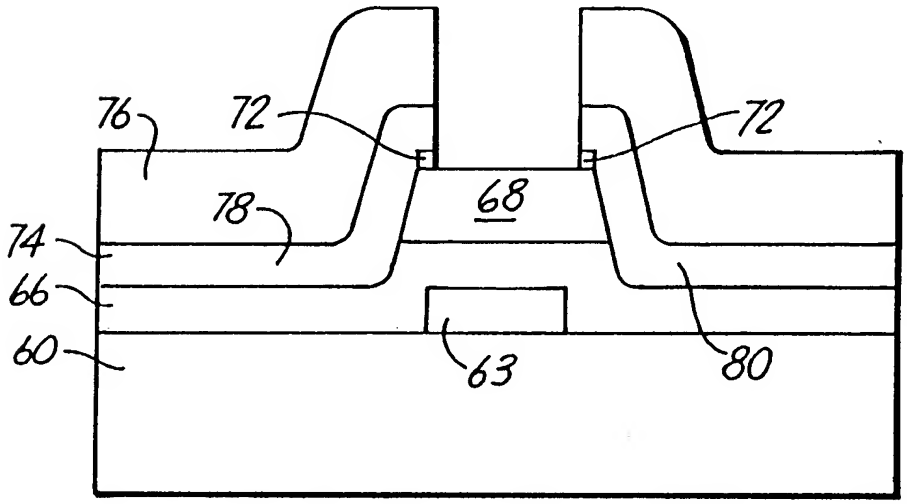

Fig. 19

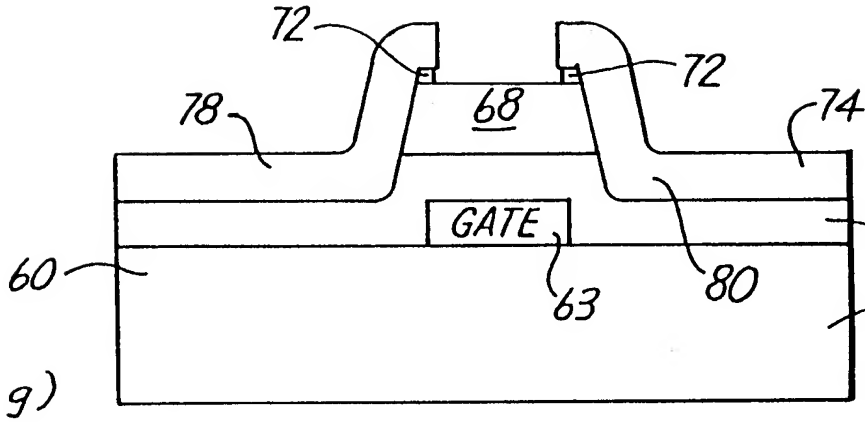
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Fig. 20

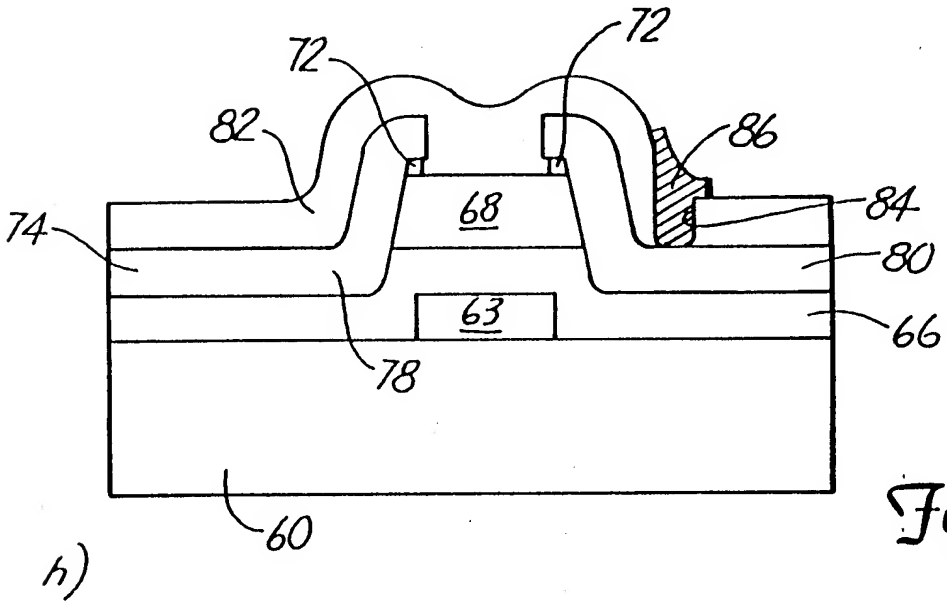
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Fig. 21

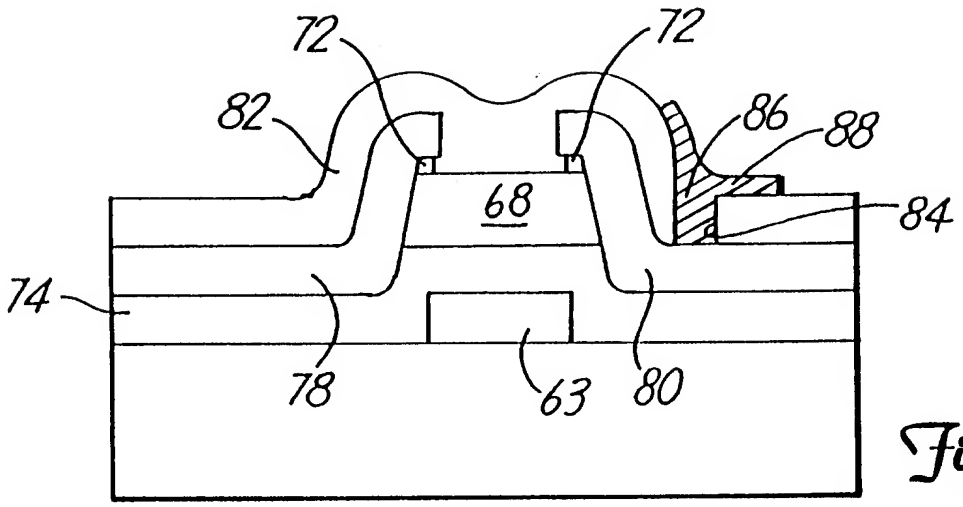

Fig. 22

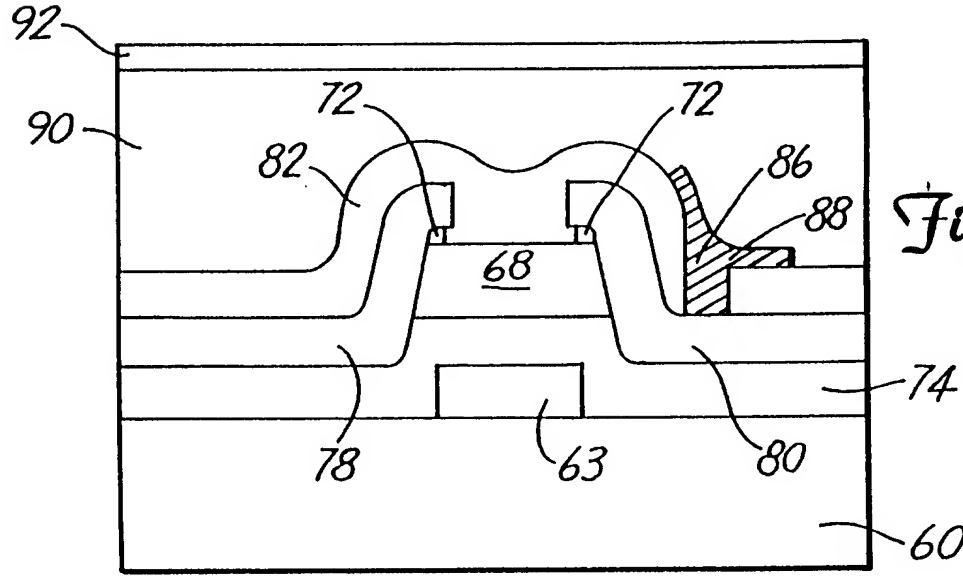

Fig. 23

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 2547

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X Y	EP-A-0 449 585 (CANON KABUSHIKI KAISHA) * page 2, line 5 - line 8 * * page 2, line 42 - line 52; figure 3 * * page 5, line 12 - page 5, line 40; figure 4 *	1,13 2,7	H01L21/336 H01L27/12
Y	PATENT ABSTRACTS OF JAPAN vol. 15, no. 280 (E-1090)16 July 1991 & JP-A-30 97 271 (RICOH CO LTD) * abstract *	2	
Y	ELECTRONICS LETTERS vol. 24, no. 3, 4 February 1988, GREAT BRITAIN pages 156 - 157 B. LOISEL ET AL. 'TWO MASK STEP POLYSILICON TFT TECHNOLOGY FOR FLAT PANEL DISPLAYS' * the whole document *	7	
A	GB-A-2 211 992 (SEKOSHA CO LTD) * page 6, line 15 - page 8, line 13; figure 1 *	1,2,7,13	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L
A	EP-A-0 377 365 (ETAT FRANCAIS) * column 7, line 41 - line 58; figure 1 *	1,2,7,13	
A A	EP-A-0 419 160 (GENERAL ELECTRIC COMPANY) * column 10, line 56 - column 11, line 15; figures 5-8 *	1,2,7,13 1,2,7,13	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 APRIL 1993	ONSHAGE A.C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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